MILLIMETRE WAVE PHASE LOCKED OSCILLATOR FOR MOBILE COMMUNICATION SYSTEMS

Isabelle Telliez - Marc Camiade - Pierre Savary - Pascale Bourne-Yaonaba

Thomson-CSF Semiconducteurs Spécifiques
RD 128 - BP 46 - 91401 ORSAY - (FRANCE)

ABSTRACT

A 56.8GHz phase locked oscillator has been developed for broadband pico-cell networks in the 62 to 63 and 65 to 66 GHz bands. A set of millimetre wave MMICs has been produced using a 0.25µm HEMT low noise process. A 10 MHz reference is used to stabilise the loop with the help of a low frequency synthesiser at 200 MHz and a sampler at 14.2 GHz. Within the temperature range 0 to 50°C, the output signals delivered at 56.8 GHz are higher than the specified 6.5 dBm ± 1.5 dB. The phase noise is better than -100 dBc/Hz at 1 MHz from carrier and lower than -70 dBc/Hz at 10 kHz from carrier. A 9 mm² multifunction chip incorporating three basic functions at 56.8 GHz has been implemented. This approach avoids critical connections and demonstrates the capability and maturity of our monolithic technology.

INTRODUCTION

For a widespread Mobile Broadband System (MBS) application, one of the most challenging issues is the development of relatively low cost transceivers. Due to critical integration problems, the GaAs MMIC's appear as a key point to carry out the millimetre-wave part for each building block. An integrated multifunction approach leads to a reduced number of chips and simplifies the assembly. The integration level will be a function of the MMIC manufacturing yield, the testing requirements and the assembly process.

The presented Millimetre-wave Phased Local Oscillator (MPLO) consists of a set of five functions developed using integrated technology for the high frequency part, a sampler for the phase comparison between the oscillator and the reference, an intermediate synthesiser at 200 MHz referenced at 10 MHz and low frequency circuits for the loop filter. The characterisation results of the device and subassemblies of the MPLO, the MPLO assembly and its overall performance are presented.

MILLIMETRE WAVE LO ARCHITECTURE

Several techniques may be used to develop a local oscillator but each one is a function of : frequency, tuning range, stability, phase noise, frequency agility (if adjustable).

Of course the cost is also a determining element and the complexity must be as low as possible. A global system optimisation has to be made in order to adapt the specifications to the chosen technology possibilities.

For MBS application, the MPLO can operate at a fixed frequency but with a very high stability. It is used for the up and down converter. Low phase noise requirements for wide band communications lead to the use of a high quality factor resonator. This approach gives very low phase noise far from the carrier (out of the frequency loop bandwidth). The stability and the near carrier phase noise, within the frequency loop bandwidth, are then only a function of the reference.

The MPLO architecture is given in fig.1. A harmonic generation has been chosen for the millimetre-wave oscillator. This approach has the following advantages:

- it allows the stabilisation of the oscillator with a well known high quality factor dielectric resonator at a half (or quarter) operating frequency.
- it is well compatible with a phase locked loop technique for the phase/frequency comparison with the reference. This comparison is generally made at oscillator frequency sub-harmonics and needs frequency division or conversion. The proposed architecture reduces the division row.

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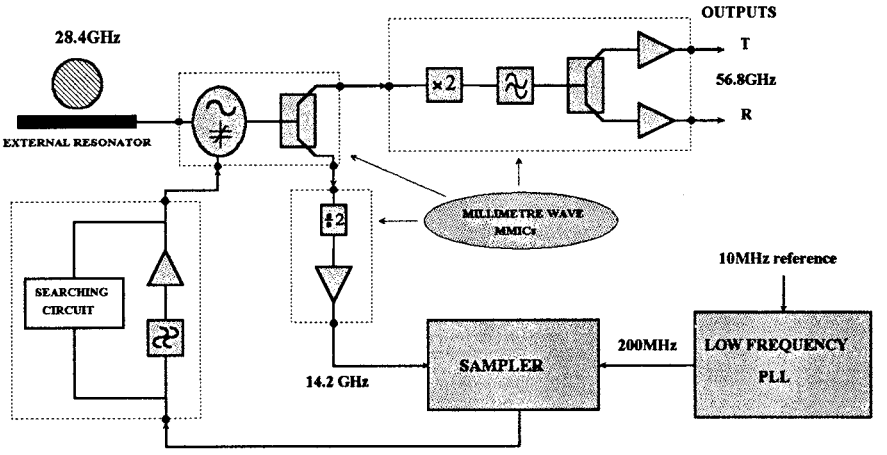

Fig.1 : Millimetre-wave Local Oscillator block diagram

The main problems of harmonic generation are the noise and the spurious signals. Therefore, a compromise has been made with an oscillator at 28.4 GHz followed by a frequency doubler and an analogue frequency divider. The filter, inserted between the doubler and the output buffer, is then easy to develop because of uncritical specifications.

A 56.8 GHz buffer amplifier/power divider provides two outputs, one for the up-converter and the other for the down-converter.

The reference is at 10 MHz and an intermediate low frequency synthesiser converts this reference to 200 MHz in order to use a snap off diode hybrid sampler at 14.2 GHz which compares the divided output frequency of the millimetre wave oscillator with the 71st harmonic of 200 MHz.

The low frequency circuits between the sampler output and the tuning voltage of the oscillator provide the main following functions:

- amplification,
- filtering in order to adjust the natural loop frequency according to the reference and the millimetre wave free running noise performances,
- searching circuit to find the frequency in the out of locking conditions. This function is necessary because a sampler is only a phase detector.

MILLIMETRE WAVE COMPONENTS

Five functions have been developed using MMIC technology:

- a Voltage Controlled Dielectric Resonator Oscillator (VCDRO) at 28.4 GHz
- a frequency doubler from 28.4 to 56.8 GHz
- a buffer amplifier/power divider at 56.8 GHz
- an analogue frequency divider from 28.4 to 14.2 GHz
- a bandpass filter.

The **VCDRO** is based on a 2*50 µm HEMT active device with a series feedback (figure 2). An essential part of this oscillator is the dielectric resonator on an adjacent alumina substrate coupled to a microstrip line, which in turn is connected, on the chip, to the gate of the HEMT. The voltage controlled tuning is achieved by a "cold HEMT" (biased at Vds=0V) used as a varactor in series with the source of the HEMT. This technique is widely compatible with the performance and allows the use of a standard technology. A buffer amplifier provides two outputs, one for the doubler and one for the divider.

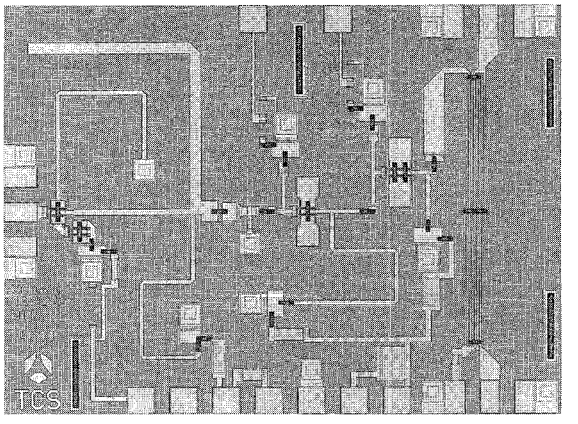

Figure 2 : Photograph of the 28.4 GHz VCDRO chip. Chip dimensions are 2 x 1.5 mm.

The measured VCDRO's have exhibited an electronic bandwidth of 10 MHz, with an output power higher than 3.5 dBm and a phase noise better than -105 dBc/Hz at 1 MHz from carrier. Temperature frequency shift is less than 3 MHz from 0 to 50°C.

The **frequency divider** is a dynamic frequency divider which uses the frequency regenerative properties of a non linear device coupled to a feed-back loop. The simplest way to carry out this loop is to use a single HEMT device whose non linearities allow to oscillate at the desired output frequency and to introduce a mixing functionality for synchronisation. As for the doubler, input and output buffer amplifiers are coupled to the divider in order to improve the isolation and the conversion (fig.3). The measurements exhibit a bandwidth greater than 12% with a centre frequency very close to the predicted value. The input power range is better than -5 to 5 dBm with an optimum value of 0 dBm. For 0 dBm input power the conversion gain is greater than 8dB with an output power of 8 dBm. These results are the best ones published until now [2].

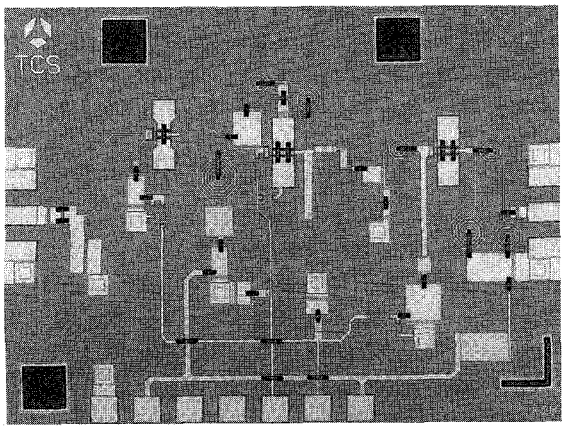

Figure 3: Photograph of the frequency divider. Dimensions of the chip are 2 x 1.5 mm.

A single ended structure has been chosen for the **frequency doubler** because it seems to be the best compromise between specifications and layout size. It consists of a 28.4 GHz input amplifier, a second stage with a HEMT biased near pinch-off for optimum second harmonic generation and an output 56.8 GHz amplifier third stage. The rejection of the fundamental frequency is obtained by the use of broadband radial stubs. Input and output amplifiers are used for buffering purposes as well as improving the conversion efficiency. The measured performances exhibit a conversion gain of 5 dB with a bandwidth higher than 7% and an output power of 5 dBm.

The **output buffer amplifier** is based on a Lange coupler followed by 3 stage amplifiers on each branch. This structure splits the input power, gives a good input matching and provides an important isolation with the previous circuit. The HEMT gate width for the last stage of each branch is 2*50 µm in order to obtain the necessary power. The chip size has been optimised by using some lumped elements instead of microstrip lines. Output power is greater than 6 dBm and the gain is higher than 10 dB.

The **filter** is a bandpass filter. It has been designed using quarter wave length coupled microstrip lines on GaAs substrate. Four sections were necessary to ensure the desired stop-band attenuation. The losses are lower than 2 dB at 56.8 GHz within a bandwidth of 20%. The rejection at 42 GHz is better than 35 dB.

MPLO INTEGRATION

All the functions, from DC to millimetre wave frequencies, are integrated in the same case. The most critical step of the assembly is the connection of RF ports of millimetre wave MMIC's. This point is fundamental because it contributes to the cost of the MPLO. The assembly cost depends of the numbers of MMIC's. A compromise has to be made between chip size, GaAs component manufacturing yield and assembly complexity. For the entire millimetre wave part of the MPLO a single chip approach seems to be the best way to reduce the RF interconnections. Indeed, a multifunction has been developed gathering the frequency doubler, the filter and the power divider/buffer amplifier (see fig. 4) with a size of 2*4.5 mm². This attempt of integration of several functions at 60 GHz in one chip fulfills the target specifications: it shows more than 6 dB conversion gain with an output power greater than 6 dBm for each output. The electrical yield of this chip is between 60% to 80% and is similar to a single function chip such as the VCDRO or the frequency divider chips. The connection between MMIC and wave guide outputs has been performed using an intermediate substrate. Bonding wires remain the simplest technique for the connection between the

chip and the substrate for small production volumes. An E-plane transition has been developed for the transition between the substrate and the wave guide. Figure 5 presents a detailed view of the microwave and millimetre-wave modules of the MPLO assembly.

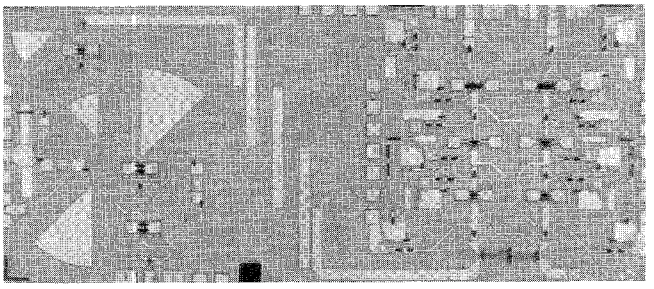

Figure 4 : Photograph of the multifunction chip.

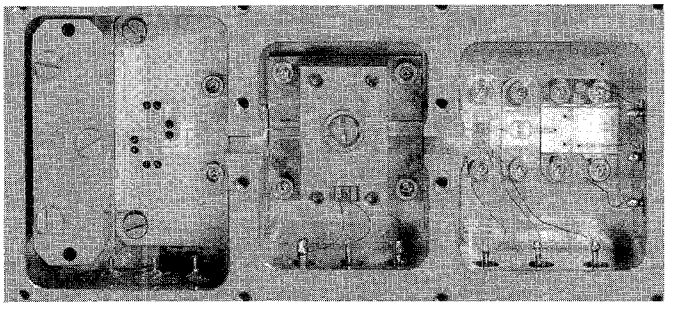

Figure 5 : Detailed view of the microwave and millimetre-wave parts of the MPLO.

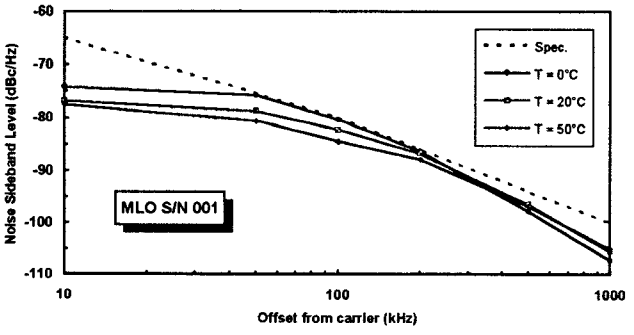

Figure 6: Phase noise variations with temperature of MLO S/N 001.

Phase noise measurement results of this assembly are presented on figure 6: the phase noise is better than -100 dBc/Hz at 1 MHz from carrier and lower than -70 dBc/Hz at 10 kHz from carrier, from 0°C to 50°C. Within this temperature range, the output signal powers delivered at 56.8 GHz are higher than the specified 6.5 dBm ± 1.5 dB range (figure 7).

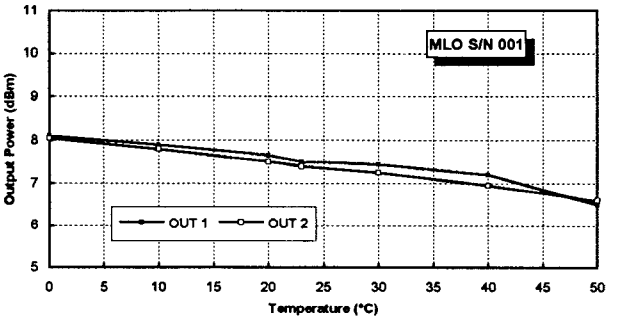

Figure 7: Output powers delivered by MLO S/N 001 vs temperature.

CONCLUSION

A 56.8 GHz phase locked oscillator has been integrated using a set of three millimetre-wave MMICs, a sampler, an intermediate low frequency synthesiser at 200 MHz and an appropriate loop filter. All the MMIC's have been successfully designed and manufactured with only one batch. The concept of multifunction approach has also been demonstrated with a 9 mm² chip including three basic functions and avoiding critical connections.

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